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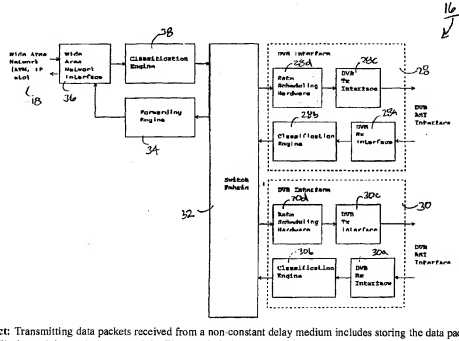
(54) Title: TRANSMITTING MPEG DATA PACKETS RECEIVED FROM A NON-CONSTANT DELAY NETWORK



(57) Abstract: Transmitting data packets received from a non-constant delay medium includes storing the data packets in a buffer (Fig 2, Ref 48), determining a play-out schedule (Fig 2, Ref 78) for the data packets based on timing information in the data packets, and transmitting the data packets from the buffer in accordance with the play-out schedule. Two of the data packets may contain time stamps and the play-out schedule may be determined based on a difference between the time stamps.

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TRANSMITTING MPEG DATA PACKETS RECEIVED FROM A NON-CONSTANT DELAY NETWORK

Cross-Reference To Related Application

This application claims priority from U.S. Provisional Application No. 60/195,850, filed April 7, 2000, the contents of which are incorporated herein by reference.

Technical Field

This invention relates generally to buffering MPEG (Motion Picture Experts Group) data packets received from a non-constant delay network and transmitting the data packets from the buffer at a determined play-out rate.

Background

Transmission of an MPEG transport stream is predicated on the use of a constant-delay transmission medium. A constant-delay transmission medium is a physical medium over which different MPEG data packets take the same amount of time to get from an MPEG transmitter/encoder to an MPEG decoder/receiver. The need for a constant-delay transmission medium is explained as follows.

clock synchronization process confuses error induced by non-constant data packet transmission with inherent error between the encoder (PCR) and receiver clocks. As a result, errors increase on average, causing unacceptably poor audio and video recovery by the MPEG decoder.

Summary

This invention enables MPEG data packets to be transmitted over non-constant data transmission media, such as a wide area network (WAN), without introducing large amounts of error into the transports stream. The invention does this by buffering MPEG data packets and reading out the buffered MPEG data packets at an appropriate play-out rate. By handling the MPEG data packets in this manner, the invention effectively mimics a constant-delay transmission medium at the receiver, thereby allowing an MPEG decoder to perform more accurate audio and video recovery. Moreover, this is done, for the most part, without altering the PCRs, thereby reducing processing time and chances for error.

In general, in one aspect, the invention is directed to a method of transmitting data packets received from a non-constant delay medium. This aspect features storing

If the play-out schedule indicates that first and second data packets are to be transmitted at the same time, timing information in the second data packet may be changed to indicate that the second data packet is to be transmitted after the first data packet. The first and second data packets may belong to first and second data streams, respectively. Timing information may be changed in other packets in the second data stream as well.

An occupancy level of the buffer may be determined and a frequency of a clock signal may be changed based on the occupancy level of the buffer. The frequency of the clock signal may be changed so that the frequency corresponds to the frequency of a clock signal that was used by a device to produce the data packets.

Other features and advantages of the invention will become apparent from the following description, including the claims and drawings.

Brief Description of the Drawings

Fig. 1 is a block diagram of a network containing an MPEG transmitter/encoder and an MPEG receiver;

Fig. 2 is a high-level block diagram of circuitry

Receiver 16 receives one or more MPEG transport stream(s), identifies individual transport stream(s), and provides audio and video output to one or more DVB (Digital Video Broadcasting) device(s) 20. The received MPEG transport streams may be transmitted by separate encoders 12 and 22 from separate sources 14 and 24, respectively. In addition, different MPEG transport streams, which originate from different sources 14 and 26, may be transmitted by the same encoder 12.

Referring to Fig. 2, a high-level block diagram of circuitry included in one embodiment of receiver 16 is shown. Receiver 16 includes two DVB device interfaces 28 and 30. Each DVB interface 28 and 30 also includes a DVB-ASI (Digital Video Broadcasting - Asynchronous Serial Interface) receive (Rx) interface 28a and 30a for receiving an MPEG transport stream, and a classification engine 28b and 30b for identifying multiple MPEG transport streams and outputting the transport streams to network 18 via switch fabric 32, forwarding engine 34, and network interface 36. The following, however, focuses first on receiving MPEG transport streams from network 18 and outputting those MPEG transport streams to DVB devices. To this end, each DVB

Classification engine 38 concatenates the virtual channel ID with a data payload contained in a data packet, any embedded time-stamps contained in the data packet, and a local time-stamp indicating the time that the data packet arrived at receiver 16. The local time-stamp is generated by classification engine 38 from a clock source (not shown in Fig. 2) on receiver 16. Switch fabric 32 uses the virtual channel ID's to associate a data packet containing a specific virtual channel ID to a switch fabric memory buffer dedicated to specific MPEG sources (e.g., sources 14 and 24 of Fig. 1) and destinations. That is, switch fabric 32 uses the virtual channel IDs to locate data associated with a particular MPEG transport stream from network 18, determine characteristics of that transport stream, and determine how that stream should be processed.

The path that the MPEG transport streams take through receiver 16 is via switch fabric 32. Switch fabric 32 can be conceptualized as a packet-aware cross-point switch. Logic implementing switch fabric 32 examines the virtual channel IDs concatenated with the incoming data packets and configures buffers and memories (e.g., buffers 40, 44, 46 in Fig. 3, described below) that are used to route the data

28d will be described). Rate scheduling logic 28d processes a set of packets 52 (Fig. 4) stored in a switch fabric memory buffer. As shown in Fig. 4, the set of packets may be a set of ten transport stream packets that do not contain PCR information (i.e., D_0 to D_9) and two transport stream packets that contain PCR information (i.e., P_0 and P_1). These latter two packets are referred to as "PCR packets" or simply "PCRs".

Rate scheduling logic 28d interprets timing information contained in the PCR packets to create a play-out schedule from the switch fabric FIFOs. Rate scheduling logic 29d reads the packets of the transport streams from the switch fabric FIFOs at the timing specified in the play-out schedule and transmits the packets to DVB Tx interface 28c. From DVB Tx interface 28c, data packet transport streams are provided to DVB device(s) 20.

In rate scheduling logic 28d, the intended bit transfer rate of a transport stream under consideration is determined by dividing the number of bits transmitted between any two PCR packets by the time difference indicated by those PCR packets. In this embodiment, the play-out rate is expressed as

for the packets scheduled between the PCRs is the correct rate. Scheduling based on PCR time differences, combined with fine control of receiver 16's output transmitter clock frequency, is employed herein to reduce network jitter.

More particularly, once an output FIFO in switch fabric 32 has accumulated half of a buffer's worth of packets, play-out starts at a nominal (predetermined) rate until the first packet containing a PCR time-stamp (P_0) is detected. After the first PCR packet (P_0) is played-out, subsequent data packets (D_4 to D_7) in the FIFO are played-out at a slightly higher rate until the next PCR packet (P_1) from that transport stream is played-out. This is done in order to reduce T_{DLY}. Reducing T_{DLY} reduces the gap in transmission between packets D_7 and P_1. Once the last packet (D_7) is played-out, FIFO play-out and transmission are suspended until the difference in time specified by the PCR packets (T_{PCR}) has elapsed. Waiting for the proper time forces the PCRs to be played-out with the proper time delay between PCRs, thereby reducing network-induced jitter. With the network jitter reduced, MPEG decoders/receivers can use normal clock synchronization processes to produce correct play-out results.

packets are thus likely to be from different transport streams. In this case, there is an opportunity for the schedule derived from the PCR information in the PCR packets to indicate simultaneous play-out. This is considered a "collision" because each receiver's output interface (e.g., 28, 30) cannot play-out two packets simultaneously. To remedy this, rate scheduling logic 28d delays the second of the two PCR packets in the play-out schedule, along with any other packets in the same MPEG transport stream as the second packet, if necessary. The time delay is equal to the time it takes for the output interface to play the previous packet. The PCR contained in the packet(s) that are delayed is compensated, i.e., changed, to account for the delay added to the schedule.

One difference between other MPEG receivers and receiver 16 is that, in receiver 16, incoming MPEG data packets are not altered except when a collision between packets occurs during "de-jittering". Other MPEG receivers modify many MPEG data packet time-stamps in an attempt to dejitter incoming data packets. Receiver 16, on the other hand, attempts to play-out each packet at its intended time rather than modifying timing information in the PCR

receiver's clock. At the point where the packet output rate matches the packet input rate, the encoder and receiver clocks are synchronized. This means that the amount of time in one count of the receiver's internal time-stamping logic matches the amount of time in one count of the encoder's time-stamping logic. Synchronization of receiver 16 and encoder 12 clocks ensures that sound and video data streams in MPEG transport streams are synchronized identically at the encoder and the receiver, allowing both audio and video to be reproduced at the receiver with relatively little error.

Referring to Fig. 3, a low-level block diagram of circuit components of receiver 16 is shown. In the embodiment shown in Fig. 3, receiver 16 contains circuitry for use with an ATM network; however, appropriate modifications permit its use with any network protocol.

SONET (Synchronous Optical Network) framer interface 58 terminates the physical layer of network (WAN) 18. SONET framer interface 58 is an actual physical interface that decapsulates ATM information mapped into a data packet payload. For the purposes of receiver 16, the SONET layer is a transparent interface. The SONET layer merely

(e.g., CAM 68) that were configured to enable processing of MPEG packets being classified. In receiver 16, the previously-configured values are derived from entries configured by a user via a user interface (not shown).

Reassembly processor FPGA 64 compares the VPI/VCI of each cell against the values in ATM virtual channel CAM 68. The comparison produces a twelve-bit VCI. The twelve-bit VCI is used by reassembly processor FPGA 64 as the address for storing payload contents of the current MPEG ATM cell in buffer dual-port RAM (Random Access Memory) 66. Each unique virtual context (meaning any cell or flow of cells identified by a unique VCI), for which cell payloads are received is stored in reassembly buffers located in buffer dual-port RAM 66. The reassembly buffers are regions of memory used to collect and assemble packets for a particular virtual channel context. In this regard, cells for a virtual context may not arrive contiguously from network 18. That is, cells may arrive that are a subset of a data segment being assembled. Received segments are thus stored so that they can be reassembled when all of the cells for their virtual context have arrived.

DVB ingress transport stream FPGA 72 classifies a packet by comparing a field, comprised of the VCI and the MPEG transport stream PID, with configured values stored in routing tag CAM 40. The comparison produces a twelve-bit routing tag. FPGA 72 replaces the ATM VCI in the prefix of the packet with this routing tag. The routing tag serves as a pointer to a packet processing descriptor that resides in dual port RAM 44. The packet processing descriptor contains information that relates to manipulating MPEG transport stream packet header information and to the switch fabric buffer destination of a data packet being processed by DVB ingress transport stream FPGA 72.

More specifically, the information in the packet processing descriptor includes one or more descriptors that instruct DVB ingress transport stream FPGA 72 to execute one or more operations on the header of a transport stream. A descriptor is a group of binary words that have specific meaning to DVB ingress transport stream FPGA 72. The descriptors include instructions to modify the current MPEG transport stream's PID, identify transport errors based on a state of a transport error indicator, identify the presence and validity of an MPEG sync-byte, identify a PCR

memory resources, such as buffer 50. Any device, including transport stream processors (e.g., 72, 74) and forwarding engines (e.g., 76, 78) that requires utilization of switch fabric buffers 48, 50 must first achieve an access grant through bus arbitration before using the switch fabric memory. Bus arbitration ensures that sequential access is maintained to the switch fabric buffers 48, 50. When the transfer by the DMA engine is finished, DVB ingress transport stream FPGA 72 modifies a relevant entry in the buffer descriptor list to indicate that switch fabric buffer 50 contains a valid packet.

Packet Forwarder/Scheduler

DVB egress FPGA 80 interrogates active entries in the buffer descriptor list and determines candidate "egress" buffers that contain MPEG data packets to be forwarded to a specific ASI transmitter 82, 84. Candidate egress buffers must satisfy certain eligibility criteria to be considered for egress. These eligibility criteria relate to the number of packets in the buffer, the type of packets in the buffer, and the validity of the buffer. For example, a buffer may be considered eligible if there are five hundred

individual DVB-ASI interface 82, 84. As noted above, the play-out schedule is determined from information contained in the PCR packets of each unique MPEG virtual context. Packet scheduler FPGA 78 determines the intended inter-arrival times of the PCR packets and determines the play-out time for a packet under consideration by referencing previously-forwarded PCR packets. Packets that do not contain PCR information are forwarded to an appropriate ASI interface with a nominal delay (T_{NOM} above) value added to their egress time.

ASI transmitter FIFO 88 (in DVB-ASI interface 84) accepts a maximum of five packets concurrently. DVB-ASI FPGA 90 monitors the occupancy of the ASI transmitter FIFO 88 and begins processing the packets as they arrive. That is, DVB-ASI FPGA 90 extracts the packets from the ASI transmitter FIFO 88 and begins to interpret the play-out schedule with relation to its internal time-base. The internal time-base is a counter that runs in sync with a 27 MHz (Megahertz) oscillator 56. When the time indicated by the internal time-base matches the time indicated for a specific packet in the play-out schedule, the packet under consideration is forwarded out of the ASI transmitter FIFO

Software Rate Control

DVB-ASI transmitters 82, 84 each contain an internal time-base reference, which is each clocked by a 27 MHz voltage-controlled oscillator (e.g., 56). This time-base, when compared to the intended packet schedule generated by packet scheduler FPGA 78, determines the play-out rate for each MPEG transport stream. The play-out rates, as noted, are determined from timing information (PCR packets - T_{PCR}) contained in the MPEG transport streams.

The MPEG encoder/transmitter time-base that generated the timing information in the MPEG PCR packets references a 27 MHz oscillator contained in the encoder/transmitter. As described above, timing errors may result because the frequency generated by 27 MHz voltage-controlled oscillator 56 does not exactly match the frequency generated by the 27 MHz oscillator(s) contained in the encoder/transmitter that generated the MPEG transport streams. These errors cause play-out from the receiver's switch fabric buffers to be slightly slower or faster instantaneously relative to the aggregate rate of the MPEG transport streams filling the switch fabric buffers. In order to compensate for this phenomenon, 27 MHz voltage-controlled oscillator 56 (and/or

center of each switch fabric buffer. The thresholds are minimum and maximum buffer occupancy marks surrounding the middle of the buffer. The center occupancy mark is reached when the buffer is exactly one-half full. In this embodiment, the two thresholds forming the minimum and maximum acceptable occupancy levels are at the one-third and two-thirds marks, respectively, of each buffer. Occupancies determined to be within the two thresholds are considered "in-range". Occupancies determined to be outside the two thresholds are considered "out-of-range".

If the average occupancy of a buffer is out-of-range, the software running in main processor 94 adjusts 27 MHz voltage-controlled oscillator 56 appropriately. That is, the 27 MHz voltage-controlled oscillator 56 is advanced if the average occupancy is above the maximum threshold. The 27 MHz voltage-controlled oscillator 56 is retarded if the occupancy is below the minimum threshold. This compensation mechanism matches the aggregate error between 27 MHz voltage-controlled oscillator 56 and the 27 MHz oscillator in the MPEG encoder/transmitter. In this manner, the frequency difference between the clocks in encoder/transmitter 12 and receiver 16 is reduced (i.e.,

ATM egress/segmentation

ATM Segmentation FPGA 76 performs a segmentation process that converts MPEG transport streams from DVB devices into the appropriate format for transmission onto network 18 as ATM cells via Utopia FIFO 77. (Reassembly is the reverse process.) The segmentation process of ATM Segmentation FPGA 76 is performed in accordance with the ATM forum AMS1.1 standard. This standard specifies the so-called 8/8 method, in which a CS-PDU comprised of two 188 byte MPEG transport streams is segmented. The CS-PDU length is 384 bytes (i.e., (2*188) + 8). The additional eight bytes are trailer information. The trailer includes a checksum, a sixteen-bit length field, and a sixteen-bit user defined field. The CS-PDU is divided into eight forty-eight-byte cell payloads. The cell payloads are then prefixed with the appropriate cell header to form transmit cells.

The MPEG packets are stored in switch fabric memory buffers 48 and 50. ATM Segmentation FPGA 76 functions as an egress processor and accesses switch fabric buffers 48 and 50 directly. ATM Segmentation FPGA 76 ensures the presence of at least two MPEG packets in a switch fabric

descriptor block can be referenced in the queue (located, e.g., dual port RAM 102 of Fig. 3) multiple times.

A ring entry location represents one transmit cell period in the transmit queue. The number and locus of entries of a descriptor block referenced in the transmit ring determines the cell rate and burstiness of the ATM cell flow. The transmit descriptor dual port RAM 8 indicates the source buffer in the switch fabric for segmentation and contains the cell header and partial context for each of sixty-four transmit threads.

The ATM cell transmission rate is determined by taking the product of the sum of valid transmit ring entries for a segmentation channel and the transmit ring entry bandwidth density. Transmit ring entry bandwidth (TREB) density is determined as follows:

$$TREB = [\#bits / ((\#entries * \#bits)/max\_cell\_rate)], \quad (2)$$

where #bits is the number of bits in a cell (424 in this embodiment), #entries is the number of entries in a ring (3000 in this embodiment), and max_cell_rate is the maximum cell rate of an OC-3 SONET interface ($132x10^6$ in this

programmed to autonomously transfer exactly one MPEG transport stream (188 bytes) to bus match FIFO 104. Main processor 94 is notified that a transfer is complete by flyby FPGA 104. Main processor 94 subsequently programs flyby FPGA 104 to transfer packets from bus match FIFO 104 to main switch fabric buffers 48, 50. The location in main switch fabric buffers 48, 50 corresponds to a queue being forwarded to/from a DVB-ASI transmitter 82, 84.

Architecture

Although receiver 16 is described primarily in a hardware context, it is not limited as such. Receiver may find applicability in any computing or processing environment. Receiver 16 may be implemented in hardware (e.g., an ASIC (Application-Specific Integrated Circuit) and/or an FPGA (Field Programmable Gate Array)), software, or a combination of hardware and software.

All or part of receiver 16 may be implemented using one or more computer programs executing on programmable computers that each includes a processor, a storage medium readable by the processor (including volatile and non-volatile memory and/or storage elements), at least one

be used with MPEG-1, MPEG-2, MPEG-4, MPEG-7, and is extendible to any other compression technique that uses the same, or similar, time-stamping mechanisms as MPEG.

Other embodiments not described herein are also within the scope of the following claims.

What is claimed is:

5. The method of claim 4, wherein the data packets that do not contain time stamps are transmitted at a higher rate in order to reduce the delay.

6. The method of claim 1, further comprising:

identifying a data stream to which the data packets belong;

wherein the play-out schedule is also determined based on the identified data stream.

7. The method of claim 6, wherein the data stream is identified based on a packet identifier in the two data packets.

8. The method of claim 7, wherein the data stream comprises an MPEG (Motion Picture Experts Group) program stream that includes audio and video information.

9. The method of claim 1, wherein, if the play-out schedule indicates that first and second data packets are to be transmitted at the same time, the method comprises:

changing timing information in the second data packet

a scheduler which determines a play-out schedule for the data packets based on timing information in the data packets; and

an interface which transmits the data packets from the buffer in accordance with the play-out schedule.

14. The apparatus of claim 13, wherein two of the data packets contain time-stamps and the play-out schedule is determined based on a difference between the time-stamps.

15. The apparatus of claim 14, wherein the play-out schedule controls play-out of the two data packets at times that correspond to the time-stamps.

16. The apparatus of claim 14, wherein data packets that do not contain time-stamps are transmitted between the two data packets such that a delay exists between a second one of the two data packets and a last one of the data packets that do not contain time stamps.

indicate that the second data packet is to be transmitted after the first data packet.

22. The apparatus of claim 21, wherein:

the first and second data packets belong to first and second data streams, respectively; and

the scheduler changes timing information in other packets in the second data stream.

23. The apparatus of claim 13, further comprising a processor that determines an occupancy level of the buffer and that changes a frequency of a clock signal based on the occupancy level of the buffer.

24. The apparatus of claim 23, wherein the frequency of the clock signal is changed so that the frequency corresponds to the frequency of a clock signal that was used by a device to produce the data packets.

25. An apparatus for transmitting data packets received from a non-constant delay network, comprising:

means for storing the data packets in a buffer;

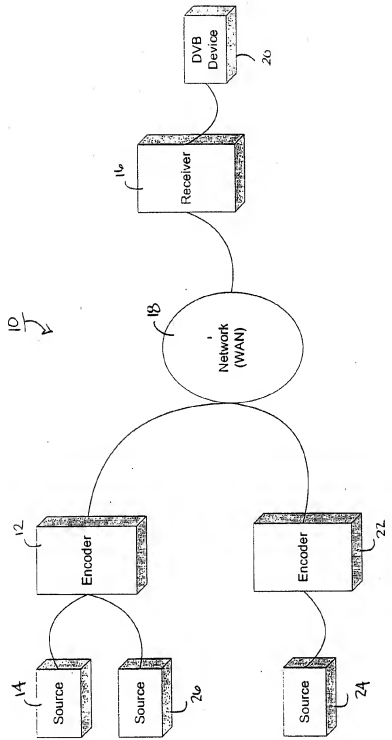

FIG. 1

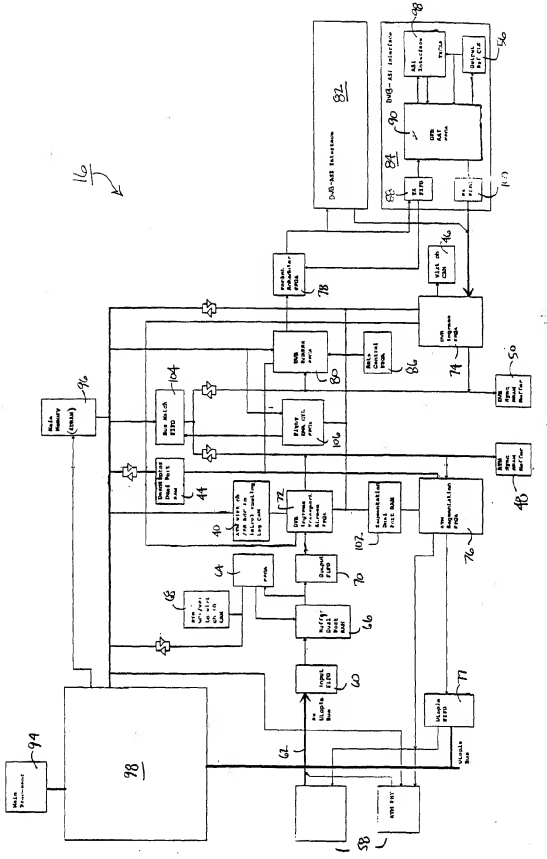

FIG. 3

INTERNATIONAL SEARCH REPORT

International application No.
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A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) : G06F 15/16; H04J 3/16
US CL : 370/350, 519, 411-418; 709/231, 205, 207

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 370/350, 519, 411-418; 709/231, 205, 207

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X,P	US 6,195,701 B1 (KAISERSWERTH et al) 27 February 2001, column 2, lines 8-17 and column 7, lines 12-20.	1-26

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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